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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,138	12/03/2003	Kaushik Saha	852463.406	5322

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/727,138	**Applicant(s)** SAHA ET AL.	
	Examiner CHAT C. DO	**Art Unit** 2193	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 10 April 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☒ The period for reply expires *3* months from the mailing date of the final rejection.
   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See below*. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-7 and 10-20*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See below.
12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

/Chat C. Do/
Primary Examiner, Art Unit 2193

Part 3(a): The applicant amended the independent claims 5 and 16 by inserting limitations "processing a digital signal" in pre-amble and "computer readable program code…storing the transformed signal" in the last line. These insertions raise new issue that would require further consideration prior marking final decision.

Part 11: the applicant argued in pages 1-2 for claims rejected under 101 rejection that the claims a practical application as processing signal on a multiprocessor system and they do not preempt every application of the ideas because they are tied to use a multiprocessing system.
The examinr respectfully submits that claims only disclose a well-known mathematical algorithm FFT in a multiprocessor system. Thus, they merely disclose the abstract/mathematical FFT algorithm without adequate specific hardware implementation. Further, they preempt every application of using FFT algorithm generally and particularly the on multiprocessor system.

The applicant argued in pages 2-3 for other claims rejected under 35 U.S.C. 101 that claim 3 as system comprises only software modules is patentable; Further claims 4 and 15 recite memory locations in the means for storing inputs and outputs and thus are directed to statutory subject matter; and Further claims 5 ad 16 are directed to a tangible medium as a computer-readable memory medium.
The examiner respectfully submits that software per se, as is seen in claim 3, which comprising only software modules are not patentable. Further, claims 4 and 15 do not disclose the means is the physical memory locations for storing inputs and outputs, but rather the processes of the means, as software module, is to store the inputs and outputs. Further, the applicant does not explicitly define the computer-readable memory medium as tangible medium as RAM, ROM, and solid semiconductor, but rather softly defines the medium as a means for storing the inputs/outputs wherein the carrier-wave is exclusively unpatentable.

The applicant argued in pages 3-4 for claims rejected under 35 U.S.C. 103(a) that the cited references by Abel et al. and Jaber fail to disclose the linear scalability as structurally disclosed in the specification (instead within the claim).
The examiner respectfully submits that the examination is mostly done on the claim language in light of the specification. Thus, the definition of linear scalability as "the computation time reducing in inverse proportion to the number of processors in the multiprocessor solution" is addressed in the original specification, but not in the claim. In addition, the step "distributing...in the stage" has no direct correlated to the definition of the "linear scalability" as "the computation time reducing in inverse proportion to the number of processors in the multiprocessor solution". Thus, the "linear scalable" is not given any patentable weight because it is recited in the preamble of the claim. In general, the combination of references by Abel and Jaber clearly discloses reasonably every single limitations cited in the claims either individually or in combination.

The applicant argued in page 4 last paragraph for claims that the current invention does not utilize the "combination phase" technique and thus it is not obvious to combine the references to meet the claimed invention.
The examiner respectfully submits that the combination of cited references by Abel et al. and Jaber discloses more detail than the current claimed invention. Thus, the combination of cited references anticipates the current claimed invention.

The applicant argued in page 5 for claims that none of references suggest or motivate a linear scalable method comprising a first radix, wherein each of the butterfly operations in each stage in the first plurality of stages has a single, un-nested computation loop of the first radix.

The examiner respectfully submits that the primary reference alone by Abel et al. discloses the above limitations as below:
Re claim 1, Abel et al. disclose in Figures 1-14 a linear scalable method for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a system (e.g. abstract, Figures 7 and 11 wherein Figure 7 discloses an IFFT and Figure 11 discloses a FFT) using a decimation in time approach (e.g. last line of abstract and col. 13 line 65 to col. 14 line 12), comprising the steps of: computing an N-point FFT/IFFT of a signal (e.g. either seen in Figures 7-8 or Figure 11 for IFFT/FFT respectively) usihg a first plurality of butterfly computational stages (e.g. Figure 4 and Figure 8 wherein the first plurality of butterfly is performed in components 800 and 805), each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix (e.g. Figure 8 wherein components 800 and 805 each utilizes radix-2 as the first radix size) wherein each of the butterfly operations in each stage (e.g. components 800, 805, and 810 in Figure 8) in the first plurality of stages has a single, un-nested computation loop of the first radix (e.g. Figure 4 and Figure 8 wherein there is no loopback/feedback for computing the IFFT/FFT); and storing the transformed signal (e.g. Figures 15-16 and col. 13 lines 10-45).